

REMARKS

Claims 1 and 3 are amended herein. Claims 10 and 12 are withdrawn from consideration. Upon entry of this amendment, claims 1-3, 10, and 12 will be pending in the above-referenced application.

Drawings

Applicants request approval of the proposed drawing changes. Specifically, the lowermost FIG. 2D has been changed to FIG. 2E, the numbering of FIGS. 3G-3J has been changed to 3A-3D, and the reference numeral 201 has been added to FIG. 6. The specification has been previously amended to reflect these drawing changes. Additionally, FIGS. 1, 3A-3D, 4, and 5 have been changed to illustrated the electrodes 17, 18 as electrically connected to the active layer 7. As discussed below, the changes to the electrodes 17, 18 in FIGS. 1, 3A-3D, 4, and 5 are supported by the specification. Applicants will submit corrected formal drawings when the above changes are approved.

Section 112

Applicants respectfully request reconsideration of the rejection of claims 1-3 under 35 U.S.C. §112, first paragraph.

The recitation of claims 1-3 of "at least one electrode extending therethrough that is operatively and electrically connected to one of said active layer, an LDD region and a source-drain region" is supported by the specification. Specifically, on page 15, lines 9-13, the specification states that "contact holes 16 are made by etching the interlayer insulating film 13 and the gate insulating film 6, as shown in FIG. 3B, and a metal, such as Al, is embedded in the contact holes 16 to form the source electrode 17 and the drain electrode 18, as shown in FIG. 3C." Because the active layer 7 including the LDD region 9 and the source-drain region 10 is sandwiched between the insulating film 13 and the gate insulating film 6, the contact holes 16 extend through the active layer and the electrodes 17, 18 are therefore electrically connected to the active layer.

Additionally, the recitation of claims 1-3 of "no etched mask structure within the thin film transistor structure" is supported by the specification. Although various masks are used to selectively etch portions of the claimed invention during formation thereof,

as shown in Fig. 1 no etched mask structures remain once formation of the claimed invention is complete.

In view of the above, the subject matter of claims 1-3 is described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Accordingly, the Section 112 rejection is improper and should be withdrawn.

Section 102

Applicants respectfully request reconsideration of the rejection of claims 1 and 2 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,281,552 (Kawasaki).

Claims 1 and 2 recite a bottom-gate thin-film transistor comprising a gate electrode, a gate insulating film, an active layer, and a protective insulating film deposited in that order on a substrate. A plurality of layers are formed over the protective film with at least one electrode extending therethrough that is operatively and electrically connected to one of the active layer, an LDD region and a source-drain region. The protective insulating film has a thickness of less than 100 nm, the protective insulating film is formed on any one of the active layer, LDD region, and source-drain region, and there is no etched mask structure within the thin film transistor structure.

Kawasaki does not disclose or suggest a bottom-gate thin-film transistor including a protective insulating film having a thickness of less than 100 nm. Rather, Kawasaki discloses a protective insulating film 150 having a thickness ranging between 100 nm and 400 nm. Accordingly, the Section 102 rejection is improper and should be withdrawn.

Section 103

Applicants respectfully request reconsideration of the rejection of claim 3 under 35 U.S.C. §103(a) as being unpatentable over Kawasaki in view of U.S. Patent No. 6,246,070 (Yamazaki).

Claim 3 recites a bottom-gate thin-film transistor comprising a gate electrode, a gate insulating film, an active layer, and a protective insulating film deposited in that order on a substrate. A plurality of layers are formed over the protective film with at

least one electrode extending therethrough that is operatively and electrically connected to one of the active layer, an LDD region and a source-drain region. The protective insulating film has a thickness of less than 100 nm, the protective insulating film is formed on any one of the active layer, LDD region, and source-drain region, and there is no etched mask structure within the thin film transistor structure.

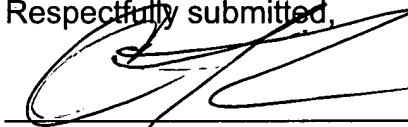
As discussed above, Kawasaki does not disclose or suggest a bottom-gate thin-film transistor including a protective insulating film having a thickness of less than 100 nm. Rather, Kawasaki discloses a protective insulating film 150 having a thickness ranging between 100 nm and 400 nm. Yamazaki does disclose an insulating film 105 and a protective film 108 having a thickness ranging between 5 and 50 nm. However, there is no motivation or suggestion within Kawasaki or Yamazaki to replace the protective insulating film 150 of Kawasaki with the insulating film 105 or the protective film 108 of Yamazaki because the films 105, 108 of Yamazaki are formed on a semiconductor film 104 before adding an impurity to the film 104 whereas the insulating film 150 of Kawasaki is formed on a silicon film 106 after doping the film 106 with an impurity element. Specifically, Kawasaki teaches away from the films 105, 108 of Yamazaki by forming a thicker insulating film 150 after the formation of impurity regions instead of adding impurities through a thinner film such as the films 105, 108 of Yamazaki to form impurity regions. Accordingly, the Section 103 rejection of claim 3 is improper and should be withdrawn.

CONCLUSION

If the Examiner believes that there is any issue which could be resolved by an interview, the Examiner is respectfully requested to contact the undersigned attorney at the telephone number listed below.

As it is believed that the application is in condition for allowance, Applicant respectfully requests a favorable action and Notice of Allowance.

Respectfully submitted,



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